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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/074,881	02/12/2002	Jiann-Tyng Tzeng	TS01-617	6517

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EXAMINER	
BROCK II, PAUL E	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 02/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/074,881	TZENG ET AL.	
	Examiner	Art Unit	
	Paul E Brock II	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 December 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 12-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 12-17* is/are rejected.

7)☒ Claim(s) *6 and 18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 December 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1 – 5, and 12 – 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al. (USPAT 6143579, Chang) in view of Yang (USPAT 5913102) and Ahn (USPAT 5563080).

With regard to claim 1, Chang discloses in the abstract and column 1, lines 19 – 36 a method for monitoring electron charge effect occurring during semiconductor processing. Chang discloses in figure 1, and column 4, line 66 – column 5, line 27 providing a substrate (10), a layer of conductivity having been created in the substrate. Chang discloses in figure 1, and column 4, line 66 – column 5, line 27 that the layer of conductivity created in the surface of the substrate is p-type. Chang does not disclose that the layer of conductivity created in the surface of the substrate is n-type. Yang discloses in figure 2, and column 6, lines 37 – 39 providing a substrate (20), a layer of n-type conductivity having been created in the surface of the substrate. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the n-type conductivity layer of Yang in the method of Chang in order to use an alternatively doped substrate as appropriate for a given process as is well known in the art. Switching conductivity

type is well known to be obvious in the art depending on the specific types of devices being fabricated. Chang discloses in figure 1 and column 5, lines 17 – 28 creating a pattern of Local Oxidation of Silicon (LOCOS) regions (12) in the substrate, the pattern of LOCOS being interspersed with exposed regions (8) of the substrate. Chang does not disclose etching the exposed regions of the substrate using the pattern of LOCOS regions as a hard mask, creating a pattern of elevated LOCOS regions, creating trenches having inside surfaces in the substrate. Ahn discloses in figures 3b – 3c etching exposed regions (17) of a substrate (11) using a pattern of LOCOS regions (16) as a hard mask, creating a pattern of elevated LOCOS regions, creating trenches having inside surfaces in the substrate. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the etching with LOCOS regions as hard masks of Ahn in the method of Chang and Yang in order to improve integration of a semiconductor device by preventing junction breakdown from occurring as stated by Ahn in column 4, lines 11 – 14. Chang discloses in figure 1 and column 5, line 28 creating a layer of interlayer oxide (14) over the pattern of LOCOS regions and the inside surfaces of the trenches created in the substrate. Chang discloses in figure 1, and column 5, lines 30 – 32 depositing a layer of polysilicon (16) over the layer of interlayer oxide. Chang discloses in figures 2a and 2b patterning (18) the layer of polysilicon, the patterned layer of polysilicon comprising at least one contact point over the substrate, completing creation of a electron charge monitoring device having a surface. Chang discloses in the abstract and column 6, lines 35 – 37 providing a semiconductor processing tool, the semiconductor processing tool being designated as being a tool being evaluated for electron charge effect of a process being performed by the tool. Chang discloses in the abstract and column 6, lines 35 – 53 positioning the substrate comprising the

electron charge monitoring device inside the processing tool in a location and a position being identical with a position and location being occupied by a substrate being processed by the tool. Chang discloses in the abstract and column 6, lines 35 – 53 establishing processing conditions of a process as these processing conditions apply for the process and the tool. Chang discloses in the abstract and column 6, lines 35 – 58 exposing the electron charge monitoring device to the established processing conditions for a period of time having a measurable duration. Chang discloses in the abstract and column 6, lines 54 – 58 terminating the processing conditions. Chang discloses in the abstract and column 6, line 60 removing the electron charge monitoring device from the semiconductor processing tool. Chang discloses in the abstract, column 4, lines 14 – 31, and column 6, line 35 – column 7, line 11 measuring voltage required to induce a FN tunneling based current between the at least one contact point of the patterned layer of polysilicon and the substrate. It should be noted that the measuring a voltage step is an intended use recitation that bears no patentable weight in a method of making claim.

With regard to claim 13, Chang discloses in the abstract and figures 1 – 2b a method of creating an electron charge effect monitoring device. Chang discloses in figure 1, and column 4, line 66 – column 5, line 27 providing a substrate (10), a layer of conductivity having been created in the substrate. Chang discloses in figure 1, and column 4, line 66 – column 5, line 27 that the layer of conductivity created in the surface of the substrate is p-type. Chang does not disclose that the layer of conductivity created in the substrate is n-type. Yang discloses in figure 2, and column 6, lines 37 – 39 providing a substrate (20), a layer of n-type conductivity having been created in the substrate. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the n-type conductivity layer of Yang in the method of

Chang in order to use an alternatively doped substrate as appropriate for a given process as is well known in the art. Switching conductivity type is well known to be obvious in the art depending on the specific types of devices being fabricated. Chang discloses in figure 1 and column 5, lines 17 – 28 creating a pattern of Local Oxidation of Silicon (LOCOS) regions (12) in the substrate, the pattern of LOCOS being interspersed with exposed regions (8) of the substrate. Chang does not disclose etching the exposed regions of the substrate using the pattern of LOCOS regions as a hard mask, creating a pattern of elevated LOCOS regions, creating trenches having inside surfaces in the substrate. Ahn discloses in figures 3b – 3c etching exposed regions (17) of a substrate (11) using a pattern of LOCOS regions (16) as a hard mask, creating a pattern of elevated LOCOS regions, creating trenches having inside surfaces in the substrate. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the etching with LOCOS regions as hard masks of Ahn in the method of Chang and Yang in order to improve integration of a semiconductor device by preventing junction breakdown from occurring as stated by Ahn in column 4, lines 11 – 14. Chang discloses in figure 1 and column 5, line 28 creating a layer of interlayer oxide (14) over the surface of the pattern of LOCOS regions and the inside surfaces of the trenches created in the substrate. Chang discloses in figure 1, and column 5, lines 30 – 32 depositing a layer of polysilicon (16) over the layer of interlayer oxide. Chang discloses in figures 2a and 2b patterning (18) the layer of polysilicon, the patterned layer of polysilicon comprising at least one contact point over the substrate. Chang discloses in the abstract, column 4, lines 14 – 31, and column 6, line 35 – column 7, line 11 measuring a voltage required to induce a FN tunneling based current between the at least one contact point of the patterned layer of polysilicon and the substrate after the substrate has been exposed to a

semiconductor processing tool under known conditions of processing by the semiconductor processing tool. It should be noted that the measuring a voltage step is an intended use recitation that bears no patentable weight in a method of making claim.

With regard to claims 2 and 14, Chang discloses in figure 1 and column 5, lines 17 – 27 creating a pattern of Local Oxidation of Silicon (LOCOS) regions in the substrate. Chang discloses in column 5, lines 20 – 22 depositing a layer of silicon nitride over the surface of the substrate. Chang discloses in column 5, lines 20 – 22 patterning the layer of silicon nitride, creating a mask of silicon nitride over the substrate, elements of the mask being interspersed with exposed regions of the substrate. Chang discloses in figure 1 and column 5, lines 17 – 27 creating layers of Local Oxidation of Silicon (LOCOS) in the exposed regions of the substrate. Chang discloses in figure 1 and column 5, lines 17 – 27 removing the mask of silicon nitride from the substrate. While Chang discloses that the LOCOS process is used, Ahn teaches other details of this well known process in figures 3a – 3c and column 2, line 52 – column 3, line 5.

With regard to claim 3 and 15, Chang discloses in column 5, lines 28 – 30 wherein the layer of interlayer is dry oxide.

With regard to claims 4 and 16, Chang discloses in column 5, lines 28 – 30 the layer of interlayer oxide being created to a thickness of 190 Angstrom.

With regard to claims 5 and 17, Chang discloses in column 5, lines 32 – 34 the layer of polysilicon being deposited to a thickness of 3,750 Angstrom.

With regard to claim 12, it should be noted that the claim limitation "the current induced between the layer of polysilicon and the substrate being 0.1 μA" is an intended use recitation. Therefore, Chang, Yang, and Ahn read on this limitation.

3. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chang, Yang, and Ahn as applied to claim 13 above, and further in view of Felch et al. (USPAT 4807994, Felch).

Chang discloses in column 5, lines 45 – 50 that a stockpile of wafers for testing are kept. Chang, Yang and Ahn are silent to the electron charge effect monitoring device can be recycled by applying an additional step of thermally annealing the substrate, thereby thermally annealing the electron charge monitoring device having been created in and on the surface of the substrate. Felch teaches in column 6, lines 15 – 36 whereby an electron charge effect monitoring device can be recycled by applying an additional step of thermally annealing a substrate, thereby thermally annealing the electron charge monitoring device having been created in and on the surface of the substrate. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the recycling step of Felch in the method of Chang, Yang, and Ahn in order to reduce costs of the monitoring process as stated by Felch in column 6, lines 15 – 36.

Allowable Subject Matter

4. Claims 6 and 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. The following is a statement of reasons for the indication of allowable subject matter: The prior art of record does not disclose or suggest, either singularly or in combination, at least the step of "the patterned layer of polysilicon comprising a square, the pattern of Local Oxidation of Silicon (LOCOS) regions comprising arrays of LOCOS regions perpendicularly and outwardly extending from each side of the square of the patterned layer of polysilicon."

Response to Arguments

6. Applicant's arguments filed December 18, 2003 have been fully considered but they are not persuasive.

7. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

8. With regard to applicant's argument that "There is in this respect no reason or motivation as to why a conductivity type that is used by Yang should be applied to the Chang et al. invention, since the Chang et al. invention at no time depends on or alludes to a conductivity type of any of the layers that are provided by Chang et al.," it should be noted that the reason given in the rejection is sufficient motivation to combine Chang and Yang. Yang is used to show that it is well known to switch conductivity types. Applicant has not given any reason why the

motivation to combine Chang and Yang fails. Further, USC 103 does not require one reference to specifically mention any aspect of the other reference for a proper combination. Therefore, applicant's arguments are not persuasive, and the rejection is proper.

9. In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E Brock II whose telephone number is (571) 272-2723. The examiner can normally be reached on 8:30 AM - 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1164. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Paul E Brock II

Tom Thomas

TOM THOMAS
SUPERVISORY
TECH